REMARKS/ARGUMENTS

The Applicants have carefully considered this application in connection with the Examiner's Action and respectfully request reconsideration of this application in view of the foregoing amendment and the following remarks.

The Applicants originally submitted Claims 1-20 in the application. In a previous response to an Election Requirement, the Applicants elected Claims 1-10 and 16-20 (representing Group II) and withdrew Claims 11-15. Presently, the Applicants have amended Claims 1, 3, 5, and 16. No other claims have been amended, canceled or added. Accordingly, Claims 1-10 and 16-20 are currently pending in the application.

I. Rejection of Claim 5 under 35 U.S.C. §112

The Examiner has rejected Claim 5 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter that the Applicants regard as their invention. Specifically, the Examiner has rejected Claim 5 as containing an antecedent basis problem. To correct this problem, the Applicants have amended Claim 5 to be dependent on Claim 4. Accordingly, the Applicants request the Examiner to withdraw the aforementioned rejection.

II. Rejection of Claims 1-3, 9-10, 16 and 20 under 35 U.S.C. §102

The Examiner has rejected Claims 1-3, 9-10, 16 and 20 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,528,327 to Nagano, *et al.* ("Nag"). Independent Claims 1 and 16

currently include the elements of removing at least a portion of residue located on an upper surface of a dielectric layer using a post planarization clean, the removing forming a recessed interconnect structure and thereby forming a recessed substrate, and conducting a recess reduction etch to reduce a relief of the recessed substrate formed by the post planarization clean. Nag fails to disclose these elements.

Nag is directed to a method for fabricating semiconductor device memory having a capacitor. (Title). Nag teaches that a conductive layer **17** located within a contact hole **16** in and over an upper surface of a passivation film **15** is polished to remove the entire conductive layer **17** from an upper surface of the passivation film **15**. Nag specifically teaches that the conductive layer **17** is over polished for a period of time about 20% to 30% longer than normally required. This over polish not only removes the entire conductive layer **17** from the upper surface of the passivation film **15**, but also creates a recess in the passivation film **15**. However, wherein Nag teaches over polishing the conductive layer **17** to form the recess in the passivation film **15**, the claimed invention requires using a post planarization clean to form the claimed recess. Therefore, Nag fails to disclose this claimed element.

Therefore, Nag does not disclose each and every element of the claimed invention and as such, is not an anticipating reference. Because Claims 2-3, 9-10 and 20 are dependent upon Claims 1 and 16, Nag also cannot be an anticipating reference for Claims 2-3, 9-10 and 20. Accordingly, the Applicants respectfully request the Examiner to withdraw the §102 rejection with respect to these Claims.

III. Rejection of Claims 4, 6-7, 17 and 19 under 35 U.S.C. §103

The Examiner has rejected Claims 4, 6-7, 17 and 19 under 35 U.S.C. §103(a) as being unpatentable over Nag in view of U.S. Pub. No. 2005/0148190A1 to Dubin, *et al.* ("Dubin"). Independent Claims 1 and 16 currently include the elements of removing at least a portion of residue located on an upper surface of a dielectric layer using a post planarization clean, the removing forming a recessed interconnect structure and thereby forming a recessed substrate, and conducting a recess reduction etch to reduce a relief of the recessed substrate formed by the post planarization clean. As previously established, Nag fails to disclose these elements. Nag further fails to suggest these elements. Specifically, because Nag teaches that its recess is formed by over polishing the conductive layer 17, Nag fails to teach or suggest that its recess is formed using a post planarization clean step, as is claimed. Thus, Nag fails to teach or suggest these claimed elements.

Dubin further fails to teach or suggest these elements. The Examiner is offering Dubin for the sole proposition of the process conditions that might be used to remove a recess. Without even addressing whether the Examiner's proposition is accurate, a teaching or suggestion of the process conditions that might be used to remove a recess is entirely different from a teaching or suggestion of removing at least a portion of residue located on an upper surface of a dielectric layer using a post planarization clean, the removing forming a recessed interconnect structure and thereby forming a recessed substrate, and conducting a recess reduction etch to reduce a relief of the recessed substrate formed by the post planarization clean, as currently claimed. Accordingly, Dubin also fails to teach or suggest these claimed elements.

Thus, Nag, individually or in combination with Dubin, fails to teach or suggest the invention recited in independent Claims 1 and 16 and their dependent claims, when considered as a whole. The combination therefore fails to establish a prima facie case of obviousness with respect to these claims. Claims 4, 6-7, 17 and 19 are therefore not obvious in view of Nag and Dubin.

In view of the foregoing remarks, the cited references do not support the Examiner's rejection of Claims 4, 6-7, 17 and 19 under 35 U.S.C. §103(a). The Applicants therefore respectfully request the Examiner withdraw the rejection.

IV. Rejection of Claims 5, 8 and 18 under 35 U.S.C. §103

The Examiner has rejected Claims 5, 8 and 18 under 35 U.S.C. §103(a) as being unpatentable over Nag in view of Dubin, and further in view of U.S. Patent No. 6,313,003 to Chen ("Chen"). As previously mentioned, independent Claims 1 and 16 currently include the elements of removing at least a portion of residue located on an upper surface of a dielectric layer using a post planarization clean, the removing forming a recessed interconnect structure and thereby forming a recessed substrate, and conducting a recess reduction etch to reduce a relief of the recessed substrate formed by the post planarization clean. As previously established, both Nag and Dubin fail to teach or suggest these claimed elements.

Chen further fails to teach or suggest these elements. The Examiner is offering Chen for the sole proposition of the process conditions that might be used to remove a recess. Without even addressing whether the Examiner's proposition is accurate, a teaching or suggestion of the process conditions that might be used to remove a recess is entirely different from a teaching or suggestion of removing at least a portion of residue located on an upper surface of a dielectric layer using a post planarization clean, the removing forming a recessed interconnect structure and thereby forming a recessed substrate, and conducting a recess reduction etch to reduce a relief of the recessed substrate formed by the post planarization clean, as currently claimed. Accordingly, Chen also fails to teach or suggest these claimed elements.

Thus, Nag, individually or in combination with Dubin and/or Chen, fails to teach or suggest the invention recited in independent Claims 1 and 16 and their dependent claims, when considered as a whole. The combination therefore fails to establish a prima facie case of obviousness with respect to these claims. Claims 5, 8 and 18 are therefore not obvious in view of Nag, Dubin and Chen.

In view of the foregoing remarks, the cited references do not support the Examiner's rejection of Claims 5, 8 and 18 under 35 U.S.C. §103(a). The Applicants therefore respectfully request the Examiner withdraw the rejection.

V. Prior Art Made of Record

The Applicants believe that the prior art made of record and not relied upon by the Examiner is not particularly pertinent to the claimed invention, but the Applicants retain the

right to address these references in detail, if necessary, in the future.

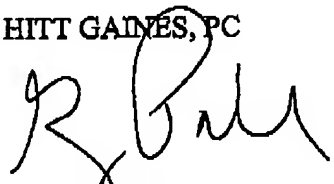
VI. Conclusion

In view of the foregoing amendment and remarks, the Applicants now see all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 1-10 and 16-20.

The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application. The Commissioner is hereby authorized to charge any fees, credits or overpayments to Deposit Account 20-0668.

Respectfully submitted,

HITT GAINES, PC



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Dated: 10-28-05

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